

PATENT

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Date: 2-2-06  
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of:

Applicant(s): Gilles Amblard, *et al.*

Examiner: Daborah Chacko-Davis

Serial No: 10/645,364

Art Unit: 1756

Filing Date: August 21, 2003

Title: COMBINATION OF NON-LITHOGRAPHIC SHRINK TECHNIQUES AND TRIM  
PROCESS FOR GATE FORMATION AND LINE-EDGE ROUGHNESS REDUCTION

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

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**STATEMENT OF SUBSTANCE OF THE INTERVIEW**

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Dear Sir:

This interview summary is in response to a telephone interview between Examiner, Daborah Chacko-Davis and Applicants' representative, Andrew R. Spriegel. Applicants' representative thanks the Examiner for the courtesies extended during the telephonic interview on December 13, 2005. The Examiner was contacted to clarify aspects of Applicants' claimed invention in

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relation to the cited references. The Applicants' representative informed the Examiner that the Singh *et al.* disclosure (U.S. 6,650,422 (Singh *et al.* '422)) cited in the Office Action dated November 2, 2005 only teaches monitoring the angular asymmetry of the planar surface, illustrated in Figs. 2a-2e. In addition, it was submitted that the system disclosed in the cited reference Singh *et al.* '422 does not teach monitoring or eliminating line edge roughness, whereas the subject claims in contrast, ***monitor line edge roughness and selectively correct line edge roughness if present***. Also the claimed invention employs a trim etch technique to compensate for any increase in critical dimension between lines on a photoresist. Although, Singh *et al.* (U.S. 6,561,706 (Singh '706)) monitors critical dimensions it does not address line-edge roughness and achieves desired critical dimensions by *controlling the exposure of the photoresist in semiconductors* and not *by trimming excess material* on the current semiconductor. Additionally the cited reference is silent with respect to ***trim techniques to maintain critical dimensions and mitigating line edge roughness***.

The applicants' representative also explained that although cited reference Arita (U.S. 6,905,949) teaches line edge roughness elimination by reflow, Arita does not teach ***monitoring line edge roughness on the photoresist, prior to reflow***. Rather, Arita teaches a post fabrication process that reflows the entire photoresist on the semiconductor, whether there is line edge roughness or not. In the claimed invention, if rework is not required, with regard to critical dimensions or edge roughness, it is not performed. The Examiner agreed to re-evaluate the cited references based upon these remarks and the formal reply to the Office Action dated November 2, 2005.

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No fee is believed to be due, but in the event any fees are due in connection with this document the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP981US].

Respectfully submitted,

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